

Amendments to the Specification:

Page 8, lines 4-17, replace paragraph [026] as amended in the Amendment filed August 19, 2005 (mail date is August 17, 2005) with the following amended paragraph:

[026] Fig. 5 shows one embodiment of the present invention, wherein a pulse generator 70 includes a TLP generator 71 and a biasing pulse source 72. The TLP generator provides a first ESD-scale pulse to first terminal 62 and a second terminal 64 of semiconductor device 60. The biasing pulse source 72 provides a second ESD-scale pulse to a second terminal 64 and a third terminal 66 of semiconductor device 60. In an embodiment wherein semiconductor device 60 is a MOS transistor, first terminal 62 and second terminal 64 are respectively a drain and a source of the MOS transistor, and third terminal 66 is the gate or substrate of the MOS transistor. In an embodiment wherein semiconductor device 60 is a SCR or LVTSCR, first terminal 62 and second terminal 64 are respectively an anode and a cathode of the SCR or LVTSCR, and third terminal 66 is the substrate or semiconductor well region of the SCR or LVTSCR. In an embodiment wherein semiconductor device 60 is a BJT or FOD, first terminal 62 and second terminal 64 are respectively a collector and an emitter of the BJT or FOD, and third terminal 66 is a base of the BJT or FOD.

Page 8, line 18 through page 9, line 2, replace paragraph [027] with the following amended paragraph:

[027] In another embodiment consistent with the present invention, the biasing pulse source 72 provides the second ESD-scale pulse to both a third and a fourth terminals of semiconductor device 60. In the embodiment in which the ESD protection device is a MOS transistor, the second ESD-scale pulse is provided to the gate and substrate of the MOS transistor. In the embodiment in which the ESD protection device is SCR or LVTSCR, the second ESD-scale pulse is provided to a substrate and a semiconductor well region of the SCR or LVTSCR.

Page 9, lines 3-6, replace paragraph [028] with the following amended paragraph:

[028] In still another embodiment, the ~~biasing pulse~~ source 72 provides the second ESD-scale pulse to a fifth terminal of semiconductor device 60. In the embodiment in which the ESD protection device is a LVTSCR, the second ESD-scale pulse is provided to a gate of a parasitic MOS transistor formed in the LVTSCR.

Page 10, line 21 through page 11, line 11, replace paragraph [033] with the following amended paragraph:

[033] If, however, no leakage current is detected, ESD-scale pulses are generated at step 104. At step 106, a first ESD-scale pulse is provided to the first terminal and second terminal of semiconductor device 60, and a second ESD-scale pulse is provided to at least the third terminal of semiconductor device 60. In one embodiment, the first and second ESD-scale pulses are generated by a TLP pulse generator. In another embodiment, the first ESD-scale pulse is generated by a TLP pulse generator, and the second ESD-scale pulse is generated by a ~~biasing pulse~~ source 72. Also consistent with the present invention, an embodiment of the present invention includes, at step 106, the second ESD-scale pulse is provided to the third terminal before the first ESD-scale pulse is provided to the first terminal and the second terminal, assisting in the determination of a point of operation of semiconductor device 60. In still another embodiment, at step 106, the second ESD-scale pulse is provided to the third terminal approximately at the same time as the first ESD-scale pulse is provided to the first terminal and the second terminal.